UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,021	09/18/2003	Robert Moss	03-0172	9135

24319 7590 01/08/2008 LSI CORPORATION 1621 BARBER LANE MS: D-106 MILPITAS, CA 95035	**EXAMINER** SHIFERAW, ELENI A

ART UNIT	PAPER NUMBER
2136	

MAIL DATE	DELIVERY MODE
01/08/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/667,021	MOSS ET AL.
	Examiner	Art Unit	
	Eleni A. Shiferaw	2136	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>*10/12/2007*</u>.

2a)☐ This action is **FINAL**.　　　2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,9-13,15 and 16* is/are pending in the application.

　　4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9-13,15 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

　　Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

　　Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

　　a)☐ All　b)☐ Some * c)☐ None of:

　　　1.☐ Certified copies of the priority documents have been received.

　　　2.☐ Certified copies of the priority documents have been received in Application No. _____.

　　　3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

　　* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
　　Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
　　Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1.   A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on 10/12/2007 has been entered. ·

2.   Claims 2, 8, and 14 are presently cancel.

3.   Claims 1, 3-7, 9-13, and 15-16 are presently pending.

Response to Amendment

4.   Applicant's arguments with respect to claims 1, 3-7, 9-13, and 15-16 have been

considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

6.   Claim1, 3-7, 9-13, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Bianco et al. USPN 5,357,572 in view of Matsui et al. 5278903.

Regarding claim 1, Bianco et al. discloses an integrated circuit (fig. 1, 3, and 6) having scan test

features (col. 2 lines 29-col. 3 lines 12) and including:

a scan test signal interceptor (fig. 1 element 14, fig. 3, element 14b, and fig. 6 element 14) for

intercepting scan test related signals applied to the integrated circuit (col. 4 lines 7-29, col. 4

lines 63-68, and col. 6 lines 17-39); and

a security element responsive to the scan test signal interceptor to preclude retrieval of

secure information within the integrated circuit using the scan test related signals (claim 1, col. 2

lines 48-58, and col. 4 lines 7-28).

wherein the security element comprises:

a reset generator to clear all secure information within the integrated circuit (see col. 6

lines 19-31, col. 5 lines 19-36, and col. 4 lines 7-28; *erasing PROM that contain each sensitive*

subcircuit).

Even though Bianco et al.'s address erasure is specifically to erase sensitive subcircuites,

as one ordinary skill in the can understands, the office herein provided Matsui et al. reference

that discloses identification information delete unit deleting identification information when a

read scan signal is detected (see col. 3 lines 54-61). Therefore it would have been obvious to one

having ordinary skill in the art at the time of the invention was made to modify the teachings of

Matsui et al. within Bianco et al. because analogous in securing data. One would have been

motivated to modify the teachings because to protect all sensitive information from being

viewed/detected during scan test signal generated.

Regarding claim 7, Bianco et al. discloses a method operable within an integrated circuit (fig. 1,

3, and 6) to prevent unauthorized access to secure information (col. 2 lines 29-col. 3 lines 12),

the method comprising:

detecting application of a scan test related signal to the integrated circuit (col. 4 lines 7-

29, col. 4 lines 63-68, and col. 6 lines 17-39); and

precluding access to the secure information in response to detection of the scan test related

signal (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28);

wherein the step of precluding includes:

resetting elements of the integrated circuit to clear all the secure information (see col. 6

lines 19-31, col. 5 lines 19-36, and col. 4 lines 7-28; *erasing PROM that contain each sensitive*

subcircuit).

Even though Bianco et al.'s address erasure is specifically to erase sensitive subcircuites,

as one ordinary skill in the can understands, the office herein provided Matsui et al. reference

that discloses identification information delete unit deleting identification information when a

read scan signal is detected (see col. 3 lines 54-61). Therefore it would have been obvious to one

having ordinary skill in the art at the time of the invention was made to modify the teachings of

Matsui et al. within Bianco et al. because analogous in securing data. One would have been

motivated to modify the teachings because to protect all sensitive information from being

viewed/detected during scan test signal generated.

Regarding claim 13, Bianco et al. discloses a system including an integrated circuit (fig. 1, 3, and 6) having a scan test capability (col. 2 lines 29-col. 3 lines 12), the system comprising:

means for detecting scan test operation of the integrated circuit (col. 4 lines 7-29, col. 4 lines 63-68, and col. 6 lines 17-39); and

means for precluding retrieval of secure information within the integrated circuit in response to detecting scan test operation (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28).

wherein the means for precluding includes:

reset means for erasing all the secure information within the integrated circuit to preclude retrieval thereof using scan test operation (see col. 6 lines 19-31, col. 5 lines 19-36, and col. 4 lines 7-28; *erasing PROM that contain each sensitive subcircuit*).

Even though Bianco et al.'s address erasure is specifically to erase sensitive subcircuites, as one ordinary skill in the can understands, the office herein provided Matsui et al. reference that discloses identification information delete unit deleting identification information when a read scan signal is detected (see col. 3 lines 54-61). Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention was made to modify the teachings of Matsui et al. within Bianco et al. because analogous in securing data. One would have been motivated to modify the teachings because to protect all sensitive information from being viewed/detected during scan test signal generated.

Regarding claim 3, Bianco et al. discloses the integrated circuit wherein the scan test signal interceptor is operable to sense a request to enter scan test (col. 3 lines 66-col. 4 lines 28).

Regarding claim 4, the combination discloses the integrated circuit wherein the reset generator is

operable to clear all secure information in response the request to enter scan test (Bianco et al.

claim 1, col. 2 lines 48-58, and col. 4 lines 7-28 and Matsui et al. see col. 3 lines 54-61).

Regarding claim 5, Bianco et al. discloses the integrated circuit wherein the scan test signal

interceptor is operable to sense a request to exit scan test (claim 1, col. 2 lines 48-58, and col. 4

lines 7-28).

Regarding claim 6, the combination discloses the integrated circuit wherein the reset generator is

operable to clear all secure information in response the request to exit scan test (Bianco et al.

claim 1, col. 2 lines 48-58, and col. 4 lines 7-28 and Matsui et al. see col. 3 lines 54-61).

Regarding claim 9, Bianco et al. discloses the method wherein the step of detecting includes:

detecting a signal applied to the integrated circuit requesting entry to scan test col. 3 lines 66-col.

4 lines 28).

Regarding claim 10, Bianco et al. discloses the method wherein the step of resetting includes:

resetting elements of the integrated circuit in response to detection of the request to enter scan

test (claim 1, col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 11, Bianco et al. discloses the method wherein the step of detecting includes:

detecting a signal applied to the integrated circuit requesting exit from scan test (claim 1, and col.

2 lines 48-58).

Regarding claim 12, Bianco et al. discloses the method wherein the step of resetting includes: resetting elements of the integrated circuit in response to detection of the request to exit scan test (col. 2 lines 48-58, and col. 4 lines 7-28).

Regarding claim 15, Bianco et al. discloses the system wherein the reset means is operable to generate a reset within the integrated circuit in response to sensing entry to scan test of the integrated circuit col. 3 lines 66-col. 4 lines 28).

Regarding claim 16, Bianco et al. discloses the system wherein the reset means is operable to generate a reset within the integrated circuit in response to sensing exit from scan test of the integrated circuit (claim 1, and col. 4 lines 7-28).
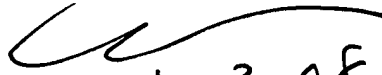
Conclusion

7.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eleni A. Shiferaw whose telephone number is 571-272-3867. The examiner can normally be reached on Mon-Fri 8:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser R. Moazzami can be reached on (571) 272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 3, 2008

NASSER MOAZZAMI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

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